1. A configurable circuit, comprising:

a variable length delay line, the delay line having an input and having N delay elements to provide a plurality of N delayed outputs;

the variable length delay line having a number of active delay elements determined by a program command; and

a configurable processing array receiving the delayed outputs from the active delay elements and secondary processing data, the configurable processing array comprising an array of configurable circuit elements.

2. The configurable circuit according to claim 1, further comprising a control processor that configures the number of active delay elements of the variable length delay line and configures the array of configurable circuit elements.

3. The configurable circuit according to claim 1, wherein the delay of the N delay elements is controlled by the control processor.

4. The configurable circuit according to claim 1, wherein the delay of the N delay elements is controlled by an output of a delay locked loop.

5. The configurable circuit according to claim 1, wherein each of the N delay elements comprises a pair of series connected inverters.

6. The configurable circuit according to claim 1, wherein the configurable processing array further comprises an input and an output that can be configured under program control.

7. The configurable circuit according to claim 1, wherein the configurable processing array further comprises a plurality of outputs that can be configured under program control.

8. The configurable circuit according to claim 1, wherein the configurable circuits comprise a plurality of configurable processing units (PUs).

9. The configurable circuit according to claim 1, wherein the configurable circuits comprise a programmable logic device.

10. The configurable circuit according to claim 1, further comprising a programmable multiplexer, responsive to the program control command to selectively enable a selected group of delay elements while disabling remaining delay elements.

11. A configurable circuit, comprising:

a variable length delay line, the delay line having an input and having N delay elements to provide a plurality of N delayed outputs;

the N delay elements each comprising a pair of series connected inverters;

the variable length delay line having a number of active delay elements determined by a program command;

a configurable processing array receiving the delayed outputs from the active delay elements and secondary processing data, the configurable processing array comprising an array of configurable circuit elements;

a control processor that configures the number of active delay elements of the variable length delay line and configures the array of configurable circuit elements; and

a delay locked loop controlling the delay of the N delay elements.

12. The configurable circuit according to claim 11, wherein the configurable processing array further comprises an input and an output that can be configured under program control.

13. The configurable circuit according to claim 11, wherein the configurable processing array further comprises a plurality of outputs that can be configured under program control.

14. The configurable circuit according to claim 11, wherein the configurable circuits comprise a plurality of configurable processing units (PUs).

15. The configurable circuit according to claim 11, wherein the configurable circuits comprise a programmable logic device.

16. The configurable circuit according to claim 11, further comprising a programmable multiplexer, responsive to the program control command to selectively enable a selected group of delay elements while disabling remaining delay elements.

17. A method of performing a circuit function, comprising:

applying an input to a variable length delay line, the delay line having an input and having N delay elements to provide a plurality of N delayed outputs, the variable length delay line having a number of active delay elements determined by a program command; and

applying the delayed outputs of the active delay elements to a configurable processing array receiving the delayed outputs from the active delay elements and secondary processing data, the configurable processing array comprising an array of configurable circuit elements that have been configured under program control to carry out a circuit function.

18. The method according to claim 17, further comprising programming the variable length delay line and the configurable processing array using a control processor that configures the number of active delay elements of the variable length delay line and configures the circuit function of the array of configurable circuit elements.

19. The method according to claim 17, further comprising controlling the delay of the N delay elements to achieve a selected overall delay.

20. The method according to claim 17, wherein the configurable processing array further comprises an input and an output that are configured under program control.

21. The method according to claim 17, wherein the configurable circuits comprise at least one of a plurality of configurable processing units (PUs) and a programmable logic device.

22. A variable delay line, comprising:

a plurality of N delay elements with each delay having an input and an output, the N delay elements being coupled together in series output to input to form a delay line;

a programming input that receives a program control command; and

a programmable multiplexer, responsive to the program control command to selectively enable a selected group of delay elements while disabling remaining delay elements.

23. The variable delay line according to claim 22, further comprising a delay control input, and wherein the delay of the N delay elements is controlled by a signal applied to the delay control input.

24. The variable delay line according to claim 23, wherein the delay of the N delay elements is controlled by an output from one of a control processor and a delay locked loop.

25. The variable delay line according to claim 22, wherein each of the N delay elements comprises a pair of series connected inverters.

26. A variable delay line, comprising:

a plurality of N delay elements with each delay having an input and an output, the N delay elements being coupled together in series output to input to form a delay line;

a programming input that receives a program control command;

a programmable multiplexer, responsive to the program control command to selectively enable a selected group of delay elements while disabling remaining delay elements; and

a delay control input, wherein the delay of the N delay elements is controlled by a signal applied to the delay control input.

27. The variable delay line according to claim 26, wherein the delay of the N delay elements is controlled by an output from one of a control processor and a delay locked loop.

28. The variable delay line according to claim 26, wherein each of the N delay elements comprises a pair of series connected inverters.